



EMBEDDED SYSTEMS DESIGN:

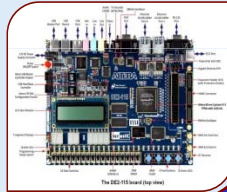


USING the ALTERA DE2-115 DEVELOPMENT AND EDUCATION BOARD

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Supervised by SFSU Graduate Student Ankita Goel and SFSU Advisor Dr. Hamid Mahmoodi

FPGA BASED EMBEDDED SYSTEM DESIGN

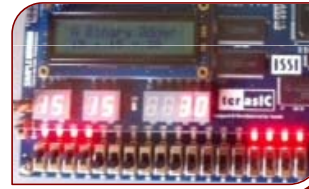
- Altera DE2-115 mounted Cyclone IV FPGA basis for programmable logic.
- Verilog used to describe hardware system.
- Architecture description language C/C++ used to describe system software.
- Codesigns utilize Nios II Soft-Core RISC processor.
- Use of IP Cores expedite generation of hardware description files.



1ST DESIGN: BINARY ADDER

Hardware-only system designed to:

- Take in binary values through two sets of slide-switches and display value on red LEDs.
- Show decimal conversion of binary value on 7-Segment Hex displays.
- Add the two binary values and display the sum on 7-Segment Hex display.
- Display all information on 16x2 Character LCD module.



FUTURE DESIGN: tPad

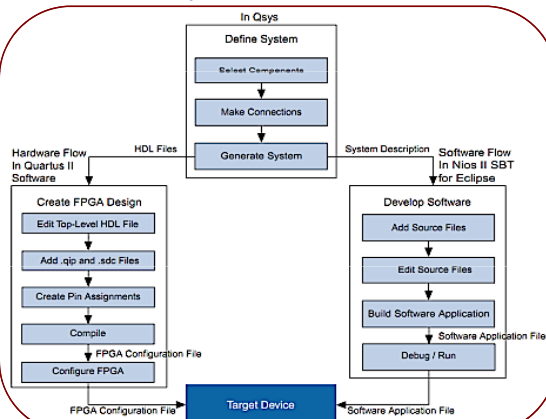
Goal: Utilize Nios II Soft-Core RISC processor in design to:

- Send continuous pixel data stream to 8" TFT-LCD with 800x600 resolution (tPad)
 - Understand required timing characteristics of LCD.
- Incorporate Altera IP Cores to generate System on Programmable Chip (SOPC).
- Develop system software description files using C/C++.



METHODS: DESIGN FLOW

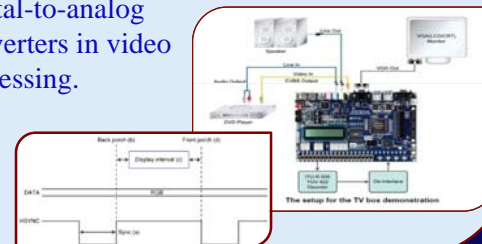
Optimized system design and implementation through partitioning of hardware description and system software.



2ND DESIGN: TV DECODER

Hardware-only system designed to:

- Convert signal from RCA output to VGA input signal for computer monitor.
- Required research:
 - Timing characteristics and implementation within hardware-only system.
 - Role and function of analog-to-digital and digital-to-analog converters in video processing.



CONCLUSIONS

- Embedded systems provide a computing advantage in real-time data processing.
 - Realized through customizable logic of FPGAs.
- Soft-core processors prevent use of unnecessary logic elements, resulting in more resource-efficient systems.
- Video streaming requires hardware specific data formatting to meet timing characteristics.
- Intellectual Property (IP) Cores allow engineers to streamline system design.
- Top-level system architecture is vital in the design and implementation of digital designs.

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