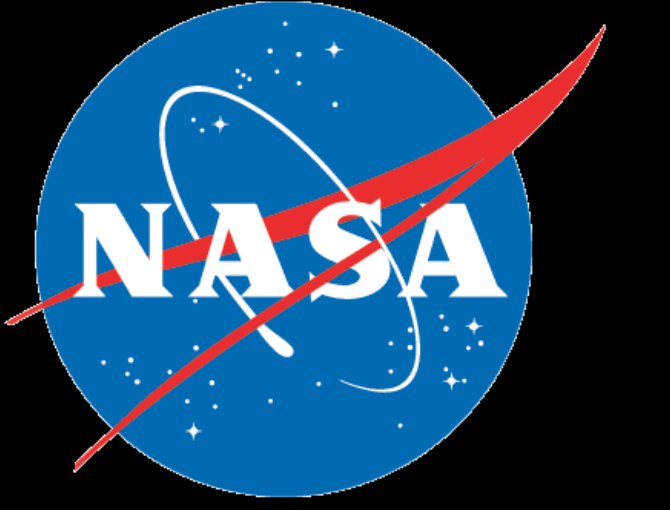


Analysis of Performance Degradation of Integrated Circuits due to Transistor Aging Effects in Nano-Scale



Jesus Garcia, Joshua Lohse, John Paulino, Hector Prado

Advisers: Hamid Mahmoodi, Amelito Enriquez, Paul Grams; Mentors: Sridevi Lakshmpuram, Atul Balani

ABSTRACT

Integrated Circuits, or ICs, work behind the scenes to improve the standard of life. IC performance dramatically improved since their first creation. However, with scaling of ICs to nano-scale, an ideal integrated circuit delivering reliable performance over its lifetime is nearly impossible. All ICs experience degradation over time due to the aging of underlying transistors. In this research, analysis of transistor breakdown is performed through computer simulations to understand effects on circuit power and performance. To simulate transistor breakdown effect, a 90nm ring oscillator circuit is utilized. This breakdown is modeled by resistors placed between the transistor terminals. This study aims to offer better insight into the impact of transistor breakdown and to improve IC design in nano-scale.

GOALS

- I. Investigate and understand Soft Oxide Breakdown (SBD) in Integrated Circuits.
- II. Gain experience in Very Large Scaled-Integration (VLSI) design software.
- III. Analyze delay multisampling feasibility.
- IV. Relate computer simulation data to experimental results.

SOFT OXIDE BREAKDOWN

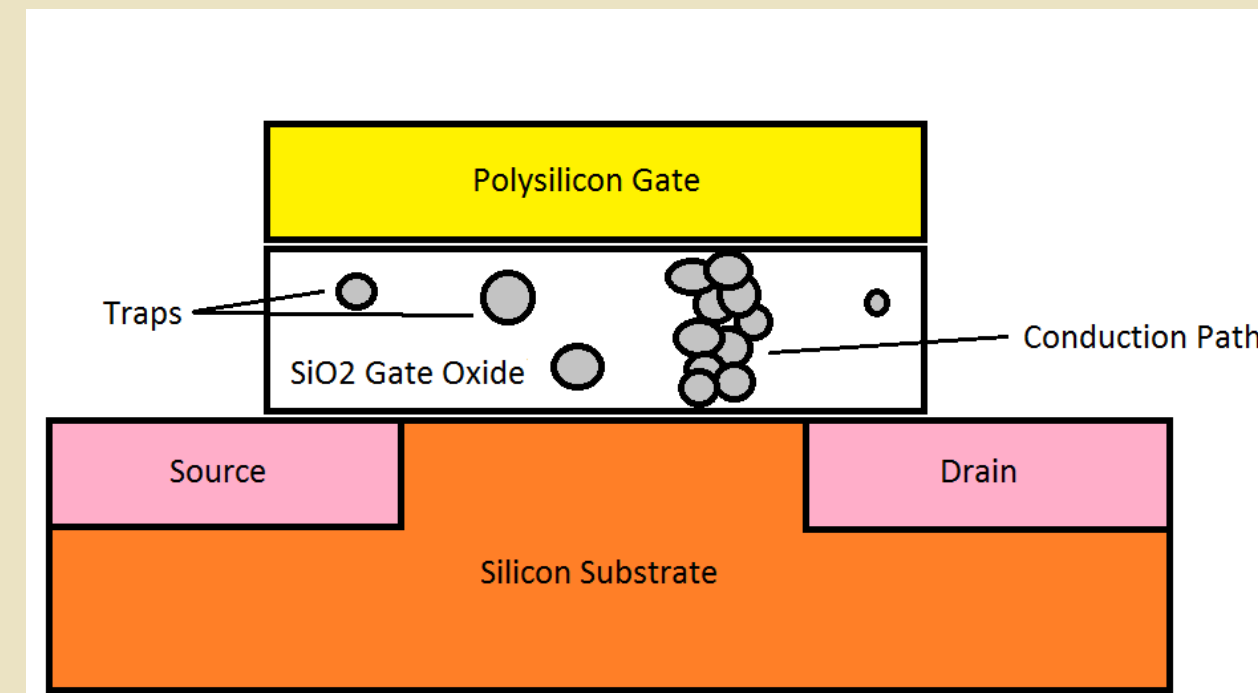


Figure 1: Cross Section of NMOS transistor showing traps and conduction path in the gate oxide region

All integrated circuits will experience degradation, which can come in many forms. SBD is a type of degradation that involves the formation of traps in the gate oxide layer of the transistor. These traps, which are defects in the structure of the SiO₂ gate oxide, form conduction paths and develop leakage current from the polysilicon gate to the silicon substrate. The leakage current affects the power consumption of the circuit even during its off state. There is debate about the cause of trap formation, which includes fabrication issues, hole creation, proton release, irradiation, and thermal damage.

APPROACH

- Model Soft Oxide Breakdown using resistance values at NMOS Gate to Source and Gate to Drain.
- Take a range of resistance values from 1MΩ down to 1kΩ and relate those values to time.
- Consider a reasonable lifetime of five years with cutoff resistance of 10kΩ.
- Use Synopsys Custom Designer for schematic design and HSPICE for running simulations.

TIME-RESISTANCE RELATIONSHIP

The resistance values which simulate SBD effect can be related to time using the equation:

$$R_{SBD} = \frac{V_{dd}}{I_0} e^{-tGR}$$

V_{dd} = supply voltage, I₀ = Initial leakage or defect current
GR = defect current growth rate, t = time

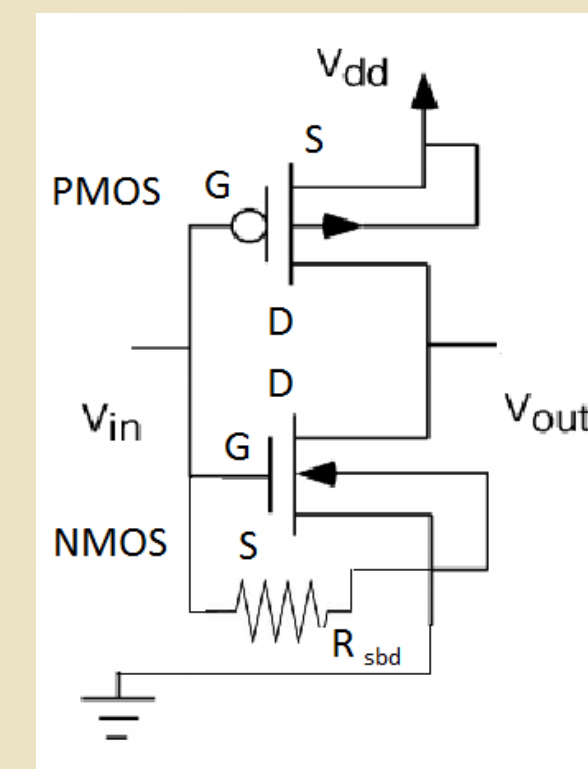


Figure 2. Transistor Symbol with R_{SBD}

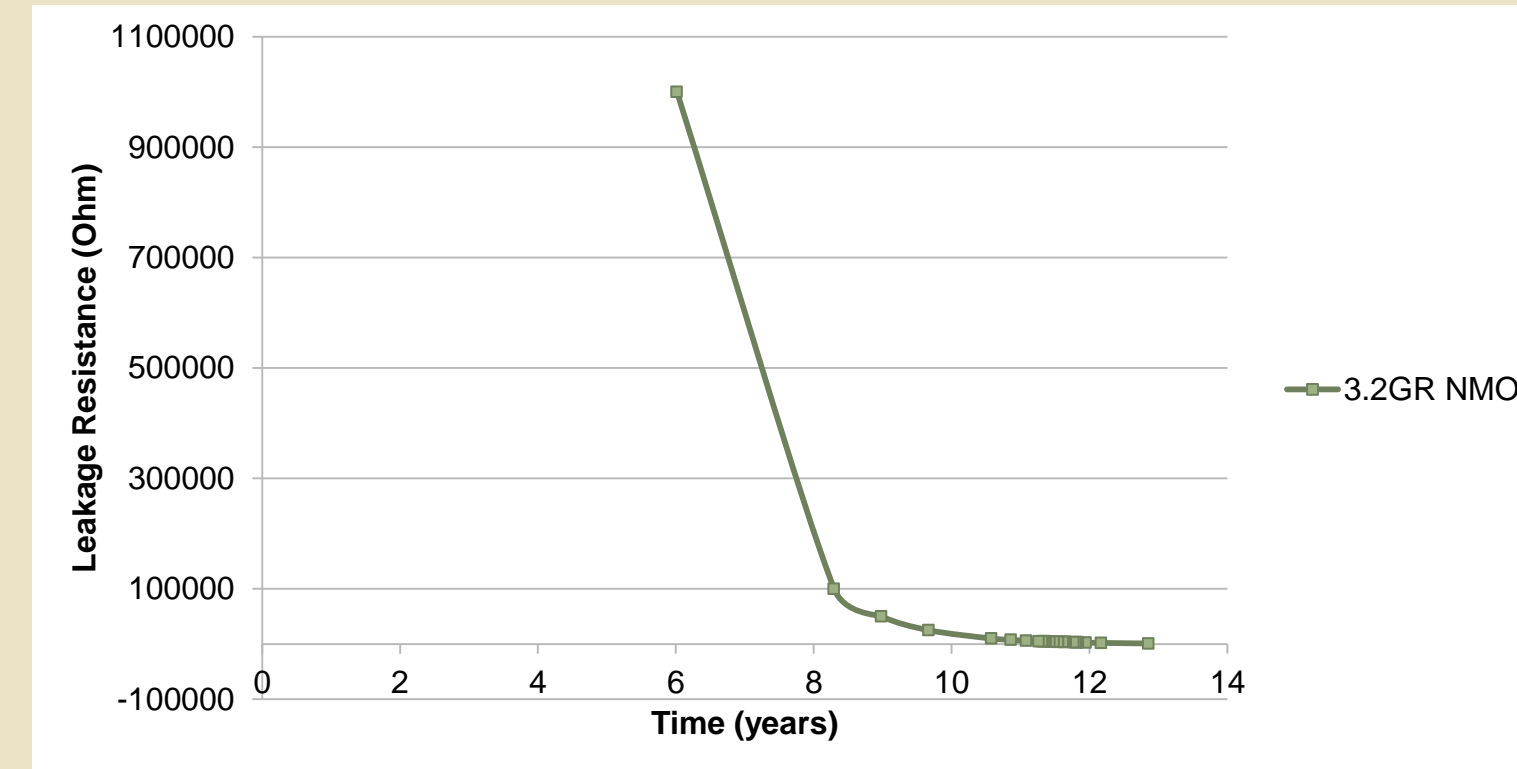


Figure 3. Resistance vs. Time Plot

ANALYSIS

A. CIRCUIT UNDER TEST: RING OSCILLATOR

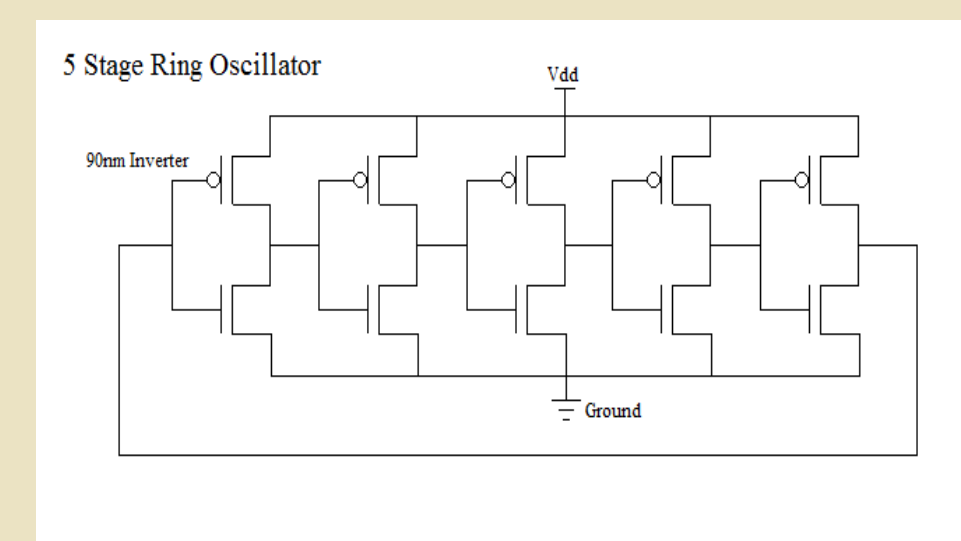


Figure 4. Schematic of 5 Stage Ring Oscillator

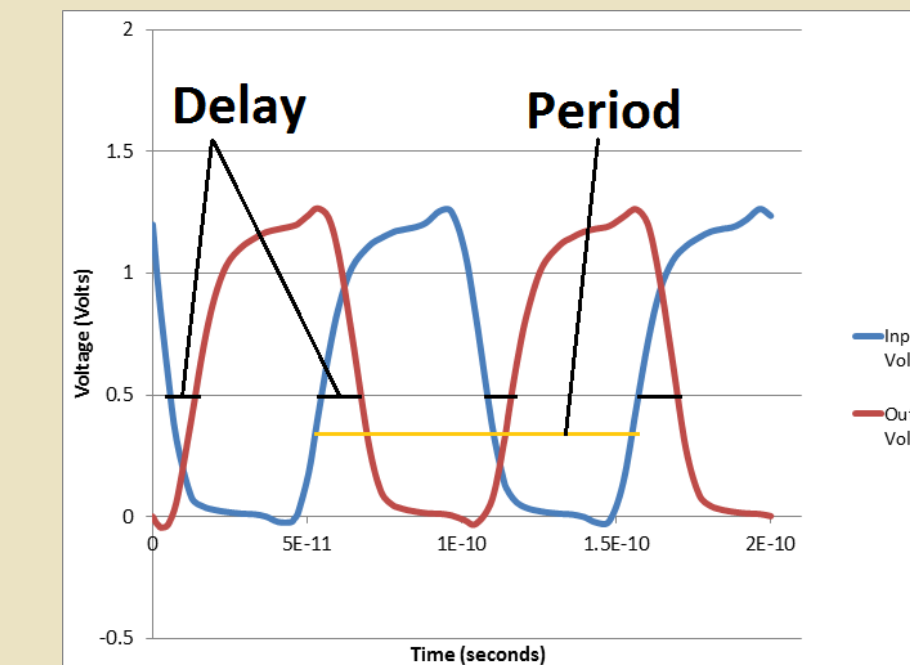


Figure 5. Input and Output Voltages of Ring Oscillator showing delay

A ring oscillator is used in place of a logic circuit for ease of design and simulation. Three ring oscillators were created in three, five and seven stages.

B. DELAY

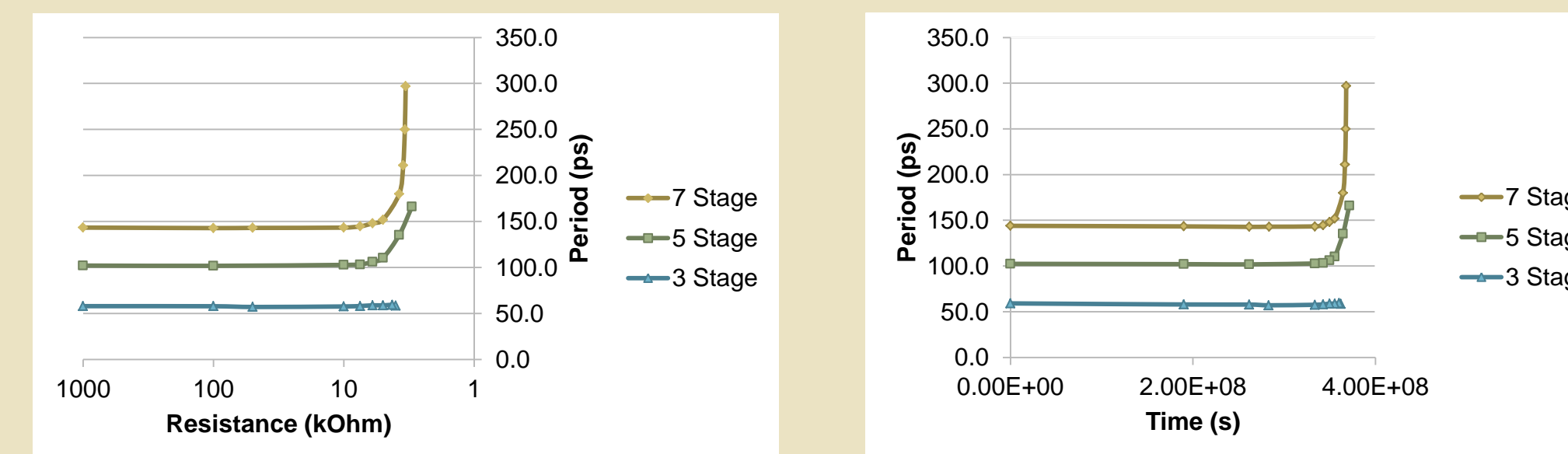


Figure 6. NMOS Gate to Source: Period vs. Resistance on left and Period vs. Time on right

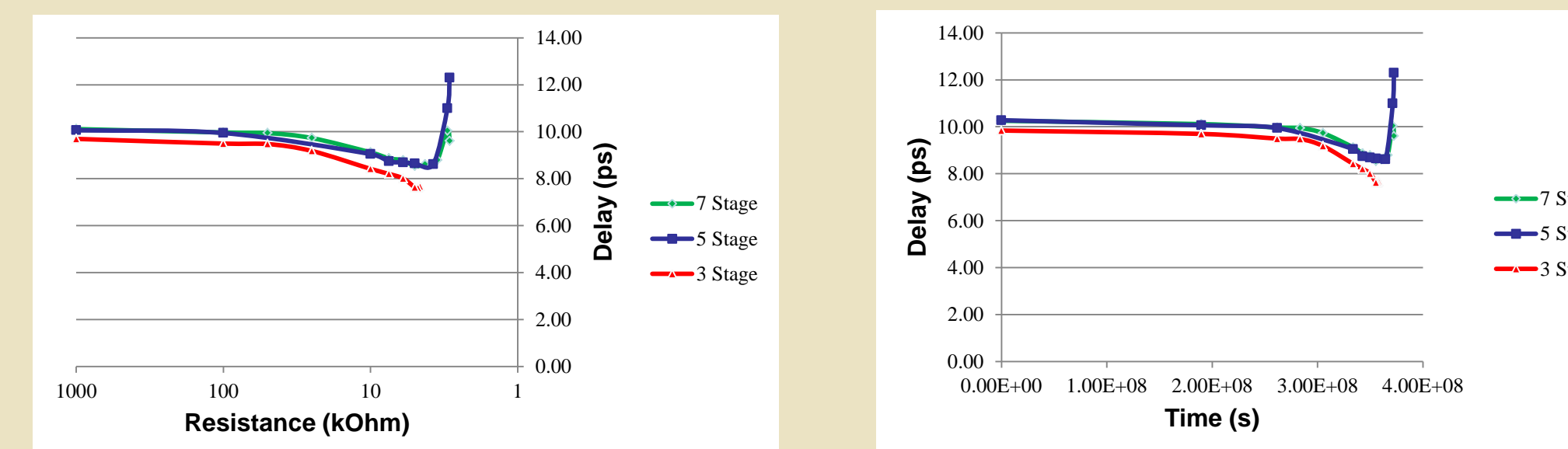


Figure 7. NMOS/PMOS Gate to Drain: Delay vs. Resistance on left and Delay vs. Time on right

PMOS/NMOS Gate to Drain shows an increase in performance until a different physical behavior called hard breakdown occurs. This breakdown causes the delay to increase exponentially.

The results from the three ring oscillators show no perceptible difference in delay up to the 10kΩ average life limit proposed in this study. Differences occur when the SBD is close to a hard breakdown ~3-4kΩ, which causes the circuit to fail completely. The differences in delay and period are believed to be too small for multisampling measurements within the confines of this study. Multisampling may be possible with simulations that have multiple inverters that suffer from SBD because they increase the delay further.

C. POWER

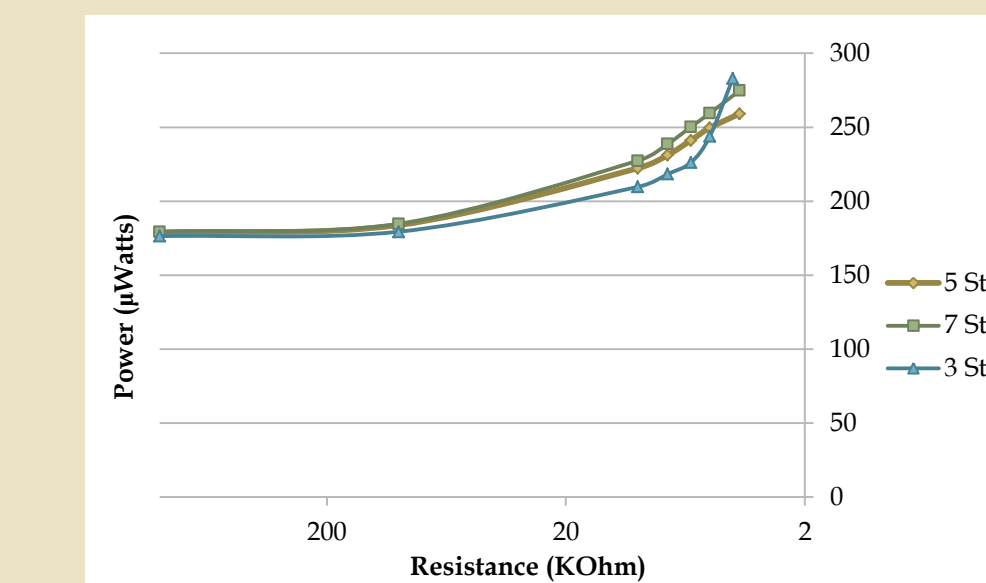


Figure 8. Power vs. Resistance

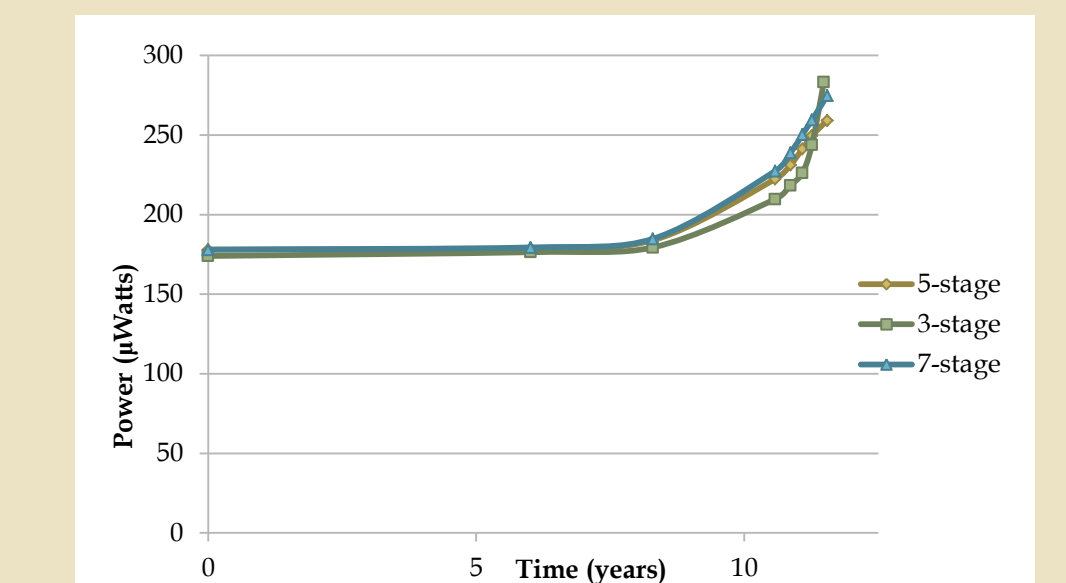


Figure 9. Power vs. Time

Figure (8) indicates that the power consumption of the circuit increases as the leakage resistance decreases because it is easier for the defect current to get through the gate oxide.

According to Figure (9), as ICs age, the power consumption mimics an exponential growth curve due to SBD.

EXPERIMENTAL RESULTS

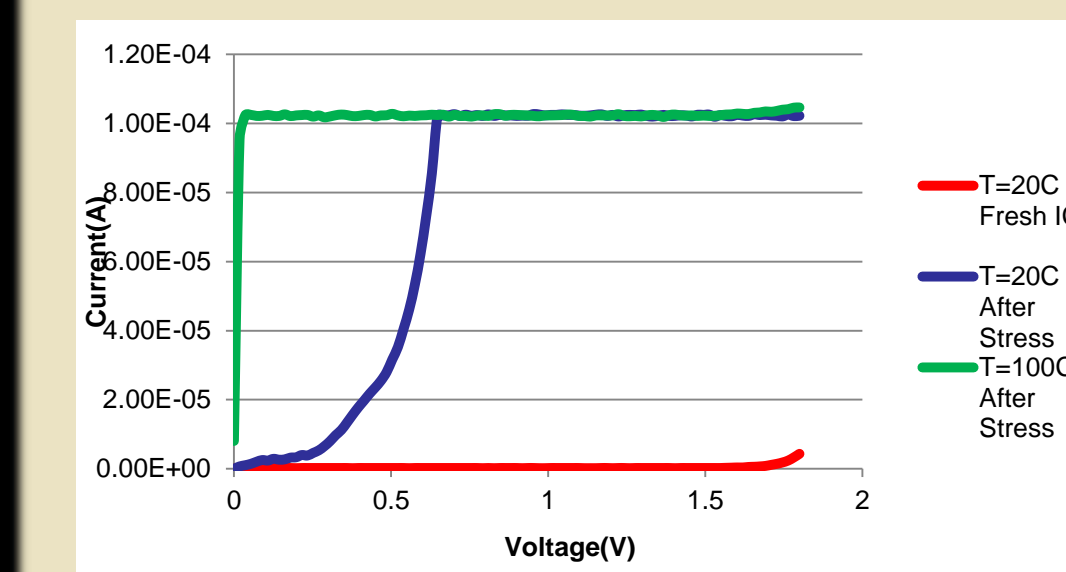


Figure 10. Current leakage measurements of Fresh IC at T=20C and stress tested IC measured at T=20C and T=100C



Figure 11. Section of chip being stress tested

The leakage vs. voltage plot of an IC before and after shows significant change as a result of breakdown after stress test.

CONCLUSION

- Adding resistors to the IC produces reliable approximations to the effects of SBD.
- SBD causes the delay to decrease under Gate to Drain breakdown, but an increase with Gate to Source.
- Delayed Multisampling is not feasible with single inverter breakdown.
- This research confirms that power consumption increases due to the increase in leakage current from SBD.
- Experimental results support our data simulations.

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